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## Radiation Testing and Evaluation Issues for Modern Integrated Circuits

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**Abstract.** Changes in modern integrated circuit (IC) technologies have modified the way we approach and conduct radiation tolerance and testing of electronics. These changes include scaling of geometries, new materials, new packaging technologies, and overall speed and device complexity challenges. In this short course section, we will identify and discuss these issues as they impact radiation testing, modeling, and effects mitigation of modern integrated circuits. The focus will be on CMOS-based technologies, however, other high performance technologies will be discussed where appropriate. The effects of concern will be: Single-Event Effects (SEE) and steady state total ionizing dose (TID) IC response. However, due to the growing use of opto-electronics in space systems issues concerning displacement damage testing will also be considered. This short course section is not intended to provide detailed "how-to-test" information, but simply provide a snapshot of current challenges and some of the approaches being considered.

## 1 Introduction

The objective of this course is to identify and discuss the issues involved with radiation testing and characterization of silicon based, deep submicron, integrated circuits and system-on-chip devices. The focus will be on single-Event Effects (SEE) with some mention of steady state total ionizing dose (TID) testing and characterization. However, due to the growing use of optoelectronics in these complex circuits displacement damage testing and characterization will also be discussed. The impact of changes in technology and circuit design issues such as circuit design complexity, operating speed, construction (e.g. number of layers of metal), packaging, circuit technology mix (e.g. digital, analog/mixed-signal, volatile and non-volatile

memory, etc) and other salient features impact testing and characterization will be identified and discussed.

Finally, recommendations to help address these issues will be provided and discussed.

## **2 Assumptions**

It is assumed that the readers of this short course have a working familiarity with basic solid state electronics technology, space radiation effects on electronics as well as the basics of radiation testing. We refer the reader to RadHome Web Site [1].

The technology covered herein is mainstream CMOS technology with only limited mention of advanced mixed signal, etc. A complete discussion of all semiconductor technologies is outside the scope of this document.

## **3 Advanced Integrated Circuit Characteristics**

### **3.1 IC Technology Advances:**

The most profound effect on SEE performance concerning future semiconductor manufacturing trends is that of feature size scaling. Scaling is too often thought of as only reducing the geometric feature size of a transistor down to 90nm and below, but is much more complex than that in reality. [Figure 1a-b ITRS Roadmap]. Technology changes may also include in new materials (e.g., alternative-K dielectrics), oxide changes, material resistivity, newer materials (e.g., SiGe), changes in interconnect structures, etc. [Figure 1c] This results in changes to device circuitry that manifest themselves as to lower operating voltages, lower nodal capacitance and higher integration density, all of which serve to increase SEU and SET sensitivity and the potential for MBU effects. In general, one can discuss the impact of these changes to radiation test and characterization as geometric or operational implications. The following sections of this document are a snapshot of radiation issues related to these scaled technologies.

**Figure 1a IRTS Roadmap**  
**Future Technology Trends**

Feature	2001	2003	2005	2007	2010	2016
Technology Node ( $\mu\text{m}$ )	130	100	70	65	45	22
Microprocessor <u>Printed</u> Gate Length ( $\mu\text{m}$ )	90	65	45	35	33	22
Microprocessor <u>Physical</u> Gate Length ( $\mu\text{m}$ )	65	45	32	25	18	9
Gate thickness (Equivalent oxide thickness nm)	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Transistor per IC (M Transistors)	97	153	243	386	773	3,093
Wafer Size (mm)	300	300	300	300	300	450
On Chip Frequency (MHz)	1,684	3,088	5,173	6,739	11,511	28,751
Number of Metal Levels	7	8	8-9	9	9-10	10
Minimum Number of Masks	24	24	26	28	28	30
Power Supply (V)	1.2	1.0	0.9	0.7	0.6	0.4
Power Dissipation (W)	130	150	170	190	218	288
Cost per Transistor (microcents/transistor)	97	49	24	12	4.3	0.5

*Source: 2001 International Technology Roadmap for Semiconductors. Values are for high performance microprocessors.*

*The values given are for high performance logic devices like microprocessors. Some of the values presented are different for low-cost, for battery-operated logic, for DRAMs and for ASICs applications.*

Figure 1b: ITRS Roadmap – CMOS Scaling

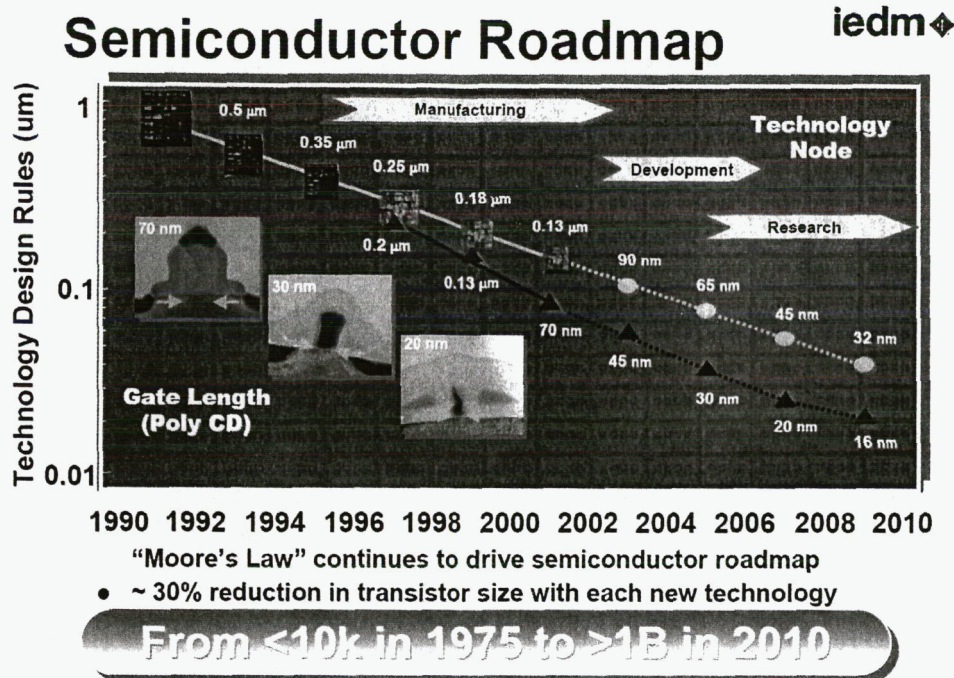
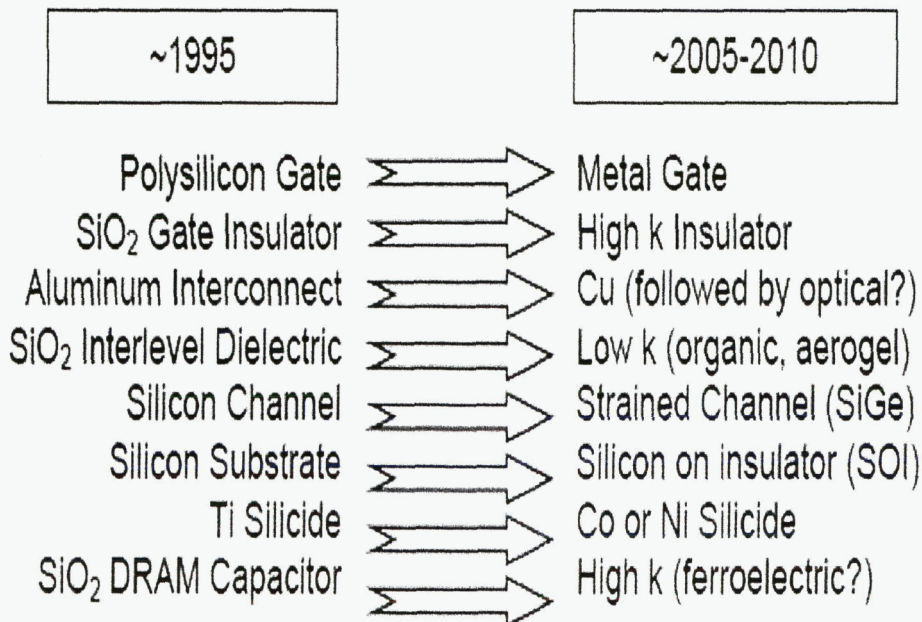


Figure 1c: IC Technology Trends

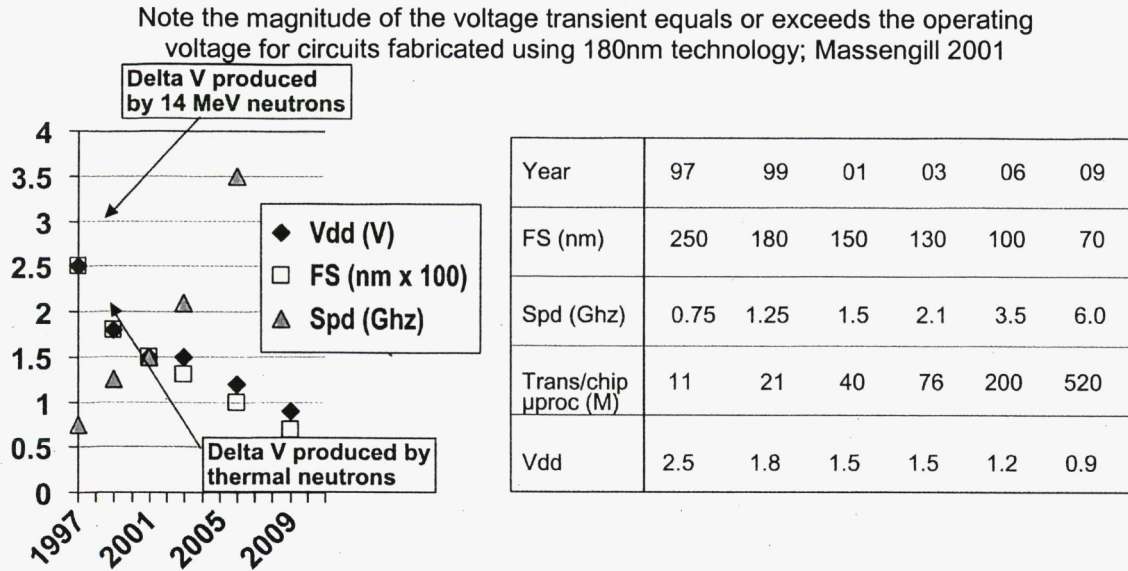
Virtually all of the Materials used to fabricate IC's in 1995 will be different in 2010  
A&T Dellin, 2005, 21st Century Semiconductor Technology



Another way to look at the effect of scaling concerning SEE is to realize that the charge deposited by an energetic particle or heavy ion is invariant and the voltage transient produced proportional to deposited charge. Thus, as we reduce the critical charge required to produce an upset (through operating voltage and nodal capacitance reductions) the sensitivity of a specific

circuit can only increase. See Figure 2 that compares the magnitude of various voltage transients to operating voltage as a function of feature size (Massengill).

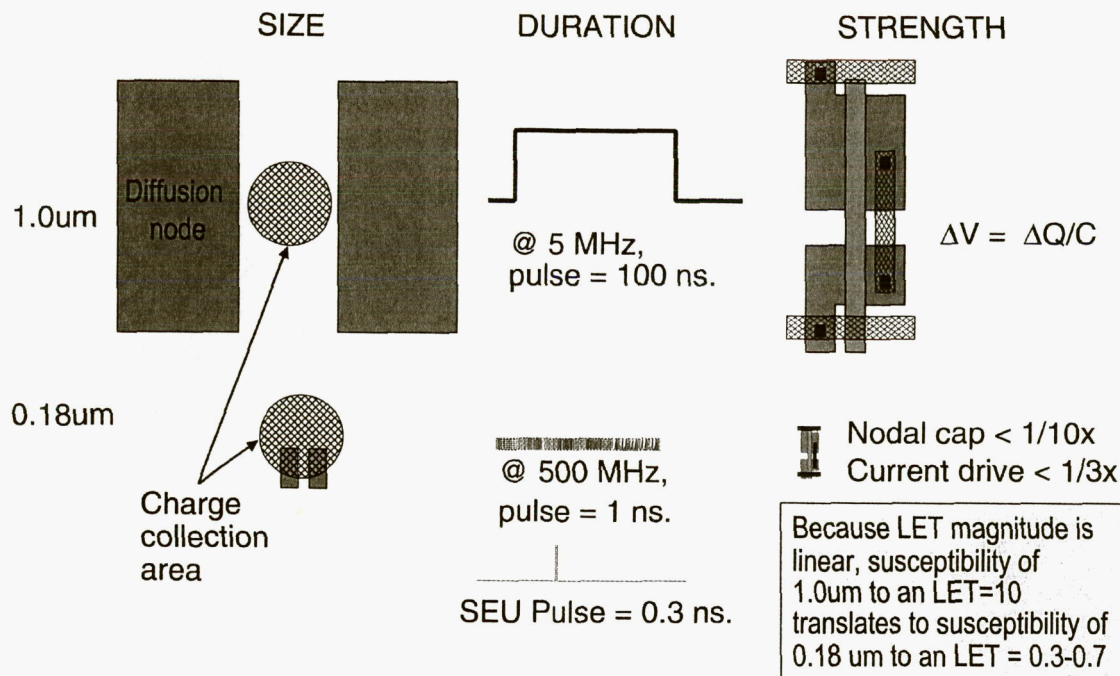
**Figure 2: Operating Voltage versus Voltage Transient Magnitude for 1MeV and 14MeV neutrons**



Another characteristic of advanced microelectronics has to do with the trend to operate at increasingly higher clock speeds and the impact of this on SET performance. The capability to operate at these higher speeds has a twofold impact in that; (1) the lower propagation delay of an individual inverter stage (or higher bandwidth) allows the voltage transients caused by particle strikes to propagate further through a multi-stage circuit without attenuation and (2) the higher clock rates provide more opportunity for a transient to be latched into a storage element (DFF or equivalent). Thus, one could postulate that there will be a cross-over point where SET induced error rate will exceed the traditional SEU error-rates as predicted by Dodd, Mavis and Benedetto, et-al.. [REF Benedetto IEEE TNS04 or SEE Symp04] [2]

Additionally, as we increase circuit density we now reach a situation where the radius of a strike now encompasses an entire memory cell or multiple transistors in the cell. This further exacerbates SEE sensitivity. [Figure 3]

**Figure 3: Comparison of the Impact of a Heavy Ion Strike for 1.0-micron and 0.18-micron Technologies, Haddad, 2000**



This issue is further complicated when we place these cell or circuit elements in closer proximity to each other, thus further increasing the probability of a multiple node strike within a circuit such as a latch. Note that even the operation of a hardened latch can be compromised if multiple nodes are simultaneously struck by a single energetic particle. This will be discussed in further detail in Section 6.

Beyond the direct ionization approach described above (charge being deposited), the ions (whether heavy ions or protons) also interact with the semiconductor as nuclear interactions causing secondary particles to be created. These secondary particles can then deposit sufficient energy to cause upsets to occur. If the sensitivity to these secondary particles scale as one would expect, device error rates will increase as well. This would require new means of predicting rates versus the industry standard CREME96 tool. The effect of these secondary particles is further exacerbated by the increasing use of high Z materials above the semiconductors active regions that contribute to the production of these particles.

Other trends that bode ill for SEE sensitivity include, but are not limited to:

- A trend away from the use of epitaxial-layered substrates
- Memory devices and microprocessors with multi-threading capability further increasing issues with SEFI and SEFI mitigation. [REF Farok Iron] [3]

As previously discussed SEL may cease to be a concern when operating voltages reach the < 1 volt range. However, until then, this failure mode must continue to be evaluated. Several trends will affect SEL sensitivity. These include:

- The trend to the elimination of epitaxial wafers for bulk designs which can further exacerbate this failure mode,
- The increasing use of SOI wafers which will serve to eliminate SEL, and,
- Asymmetry of device layouts.

In a recent paper provided at the IEEE IRPS (Bose 2005) a comprehensive study of electrically induced latch-up was conducted for four generations of IC's (180, 130, 90 and 65 nm CMOS technologies and concluded that scaling trends have resulted in reduction of intrinsic

process sensitivity to latch-up, however the performance boosts resulting from scaling are promoting the potential for enhanced latch-up stimuli. Factors such as faster signal transitions and slew-rates promote higher displacement currents, new complex testing requirements have been reported to have caused latch-up failures (Chatty 2004) and the smaller distances between pads can also engender latch-up (Sal 2004). Finally, neutron induced latch-up has been seen in SRAM's at a ground level (Vold 2004).

### 3.2 Circuit-level Advances

Other considerations affecting the utilization, testing and characterization of advanced IC's related to the increased functionality and design complexity associated with these devices to include the following attributes:

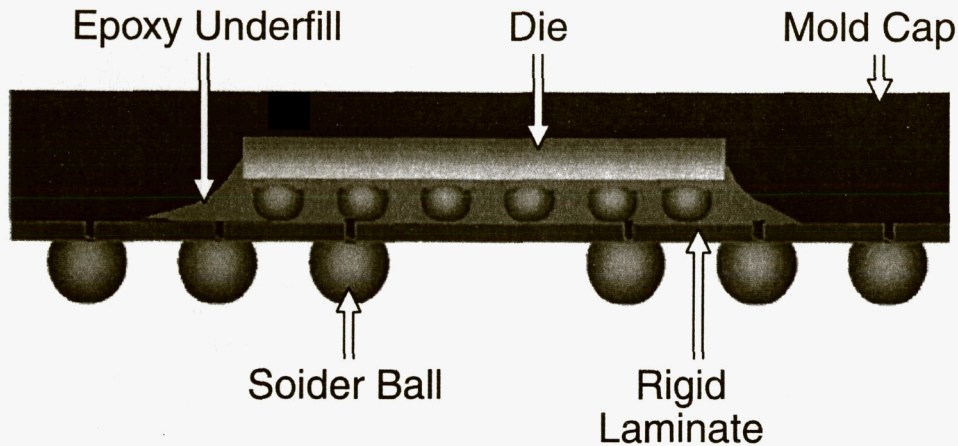
- **Intelligence:** Circuits contain embedded microprocessors, microcontrollers, programmable fabric and other circuits that allow some degree of autonomous operation and a variety of operating configurations that must be evaluated. This attribute also makes the identification and selection of an appropriate set of test vectors and fault coverage difficult. Also, many of these devices have built in fault protection, e.g. EDAC, voting schemes, etc., that can affect testing and error-rate prediction.
- **Flexibility or programmability:** Circuits are being constructed with embedded SRAM or EEPROM based programming capability that can be upset such that the architecture configuration of a circuit is lost or rearranged. This attribute can effect the approach to testing and characterization for both SEU and TID depending on the storage mechanism.
- **Complexity:** Circuits are comprised of a variety of different circuit types and possibly technologies with different failure modes and sensitivities that include, but are not limited to, CMOS digital logic and volatile memory; floating gate or some other type of non-volatile memory (e.g. EEPROM, FERAM, C-RAM, etc.); CMOS analog/mixed-signal circuits (e.g. ADC, DAC, SERDES, LVDS, voltage references, etc.), opto-electronic couplers and others. This complexity impacts error-rate predictions due to the various sensitive cross-sections and linear energy transfers (LETs) that are involved with an IC, test performance, test facility and test beam selection and a variety of other specific testing considerations.
- **Integration density:** Circuits are comprised of literally millions of critical nodes making fault coverage and test vector selection difficult. Also, the issue of MBU concerning error-rate predictions is affected by this factor.
- **Hidden Circuit Features:** Circuits often have many thousands of registers, built-in test elements, and other embedded circuits that are not identified by the manufacturer but can influence the radiation response of the overall device. These areas of the device may not be accessible to the external user.
- **Multi-layered construction:** Circuits are often fabricated using many levels of metal and complex packaging that make the interrogation of critical nodes using most SEE test facilities difficult if not impossible. These construction methods also preclude the use of diagnostic tools such as lasers or ion-micro beams. In addition, concerning SEE testing the over-layers can contribute secondary particles that influence the radiation response and make error-rate prediction difficult. Finally, these metal layers and other construction methods such as the use of high Z metals can cause dose-enhancement effects that are difficult to predict but have the potential to impact circuit lifetimes in a steady state TID radiation environment.
- **Power Requirements:** Circuits run "hot", consuming significant amounts of power, that make testing in a vacuum or other restricted spaces very difficult.
- **Speed of operation:** The high operating speeds of these circuits require that SEE testing at or near the intended operating speed of the device be accomplished to obtain

conservative error-rate estimates. For typical SEE test set-ups that require relatively long cabling this requirement poses a significant problem.

### 3.3 Packaged Component Trends

These are several factors concerning packaging that have further complicated our ability to perform SEE testing and characterization. The most salient of these includes; (1) the use of plastic encapsulation and (2) the transition from relatively simple ceramic in-line packages to complex methods such as flip-chip ball grid array (FC BGA) packages.

**Figure 4: FC BGA**



Plastic encapsulation has significantly complicated device SEE test preparation since removal without damaging the DUT can be a time consuming and difficult endeavor. [ref JPL NASA doc] [4]

The issues associated with the use of FC BGA package technology, however, are more profound due to inherent SEE test facility beam energy limitation. Although there are a few exceptions, the primary SEE facilities cannot provide sufficiently energetic beams to penetrate these complex packages and thus, significant effort is required to prepare the DUT via substrate thinning, package modification or complete re-packaging.

In subsequent sections of this course, the impact of the above noted attributes will be discussed with respect to their effect on device radiation response characterization and the adequacy of the test and characterization infrastructure to meet the demands imposed by them.

## 4 Representative Radiation Test and Modeling Issues Engendered by Advances in IC Technology

In this section we will examine the impact of the characteristics and attributes of these advanced microelectronic devices concerning radiation testing, modeling and simulation.

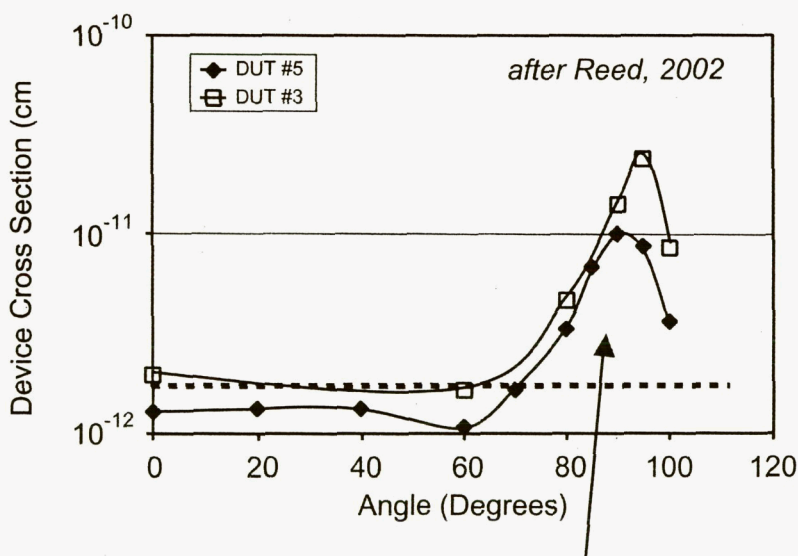
These impacts or issues can be grouped into several categories that include:

- **Device physics:** In this category, issues such as 3-D charge collection and generation modeling and simulation in highly scaled devices, the impact of secondary generation on SER, limitations in sensitive volume assumptions, angular strike response and other issues associated with the present state-of-our understanding of the basic mechanisms associated with ionizing radiation effects in ultra-deep-submicron semiconductor electronics. Examples of issues that highlight shortfalls in the present knowledge base are shown in Figures 5 (showing

unanticipated directionality effects from proton interactions in SOI technologies) and 6 (showing anomalous charge collection in SiGe devices) where discrepancies between anticipated and actual test results are depicted.

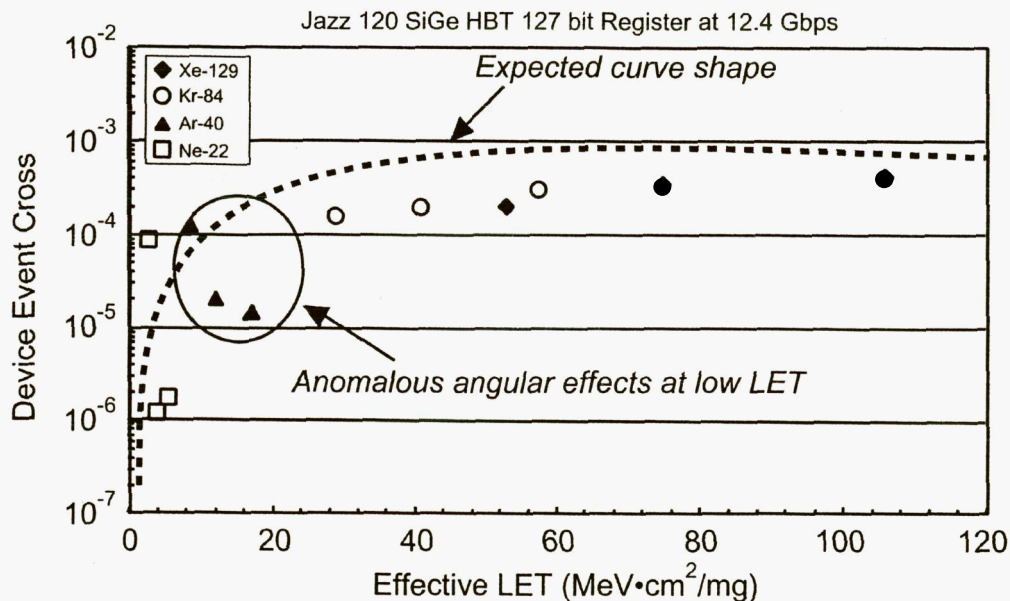
- **Radiation testing issues including test implementation and test facility limitations:** At present the traditional methods concerning the implementing SEE testing impose severe limitations WRT obtaining a conservative characterization of the radiation response of advanced IC's. Simply stated the need to test at realistic clock speeds, commensurate with actual IC operation, is not possible using the traditional approach that rely on bringing signals in and out of the DUT through long cables. Signal, thermal, power, device and cable I/O, and data capture are among the more intrusive issues with the traditional approach versus these newer technologies. Thus, more elegant on-chip or onboard test techniques and circuits must be developed and validated (Mars 05) that actually include the test signal generation and some the capability to capture and/or partially reduce the raw test data.

**Figure 5: Effects of Protons in SOI**



Effects of protons in SOI with varied angular direction of the particle;  
Dashed line represents expected response with "standard" CMOS devices.

**Figure 6: Effects of Heavy Ions on SiGe Devices**



Effects of heavy ions on SiGe devices at 12 GHz speeds notes anomalous charge collection of this high-speed technology;  
 Drawn line represents expected response with "standard" models.

In general test facility limitations are the result of the increasingly complex packaging systems that are being employed to support advanced IC's where > 1000 input/output pin counts are needed. The material systems and configuration of these packages provides a twofold deleterious effect concerning SEE testing and performance where; (1) the thickness of the package and inverted insertion of the chip greatly attenuate the beam LET making conservative testing impossible (except for a few facilities) and, in addition, (2) the high-Z materials generate secondary particles that contribute to the SER as a function of beam energy

- **Modeling and Simulation Limitations:** As previously stated the disparity of the results between modeled and measured SEE response (REF Schrimpf/Reed/Weller HEART 05) [5] strongly suggest that our ability to model radiation effects in complex IC technology is severely limited. Specific areas of concern include the basic limitations and inaccuracies associated with existing transistor SPICE models, physics based TCAD models and the compact radiation effects models derived from the test data and/or the more complex physics models.

## 5 Test Methods

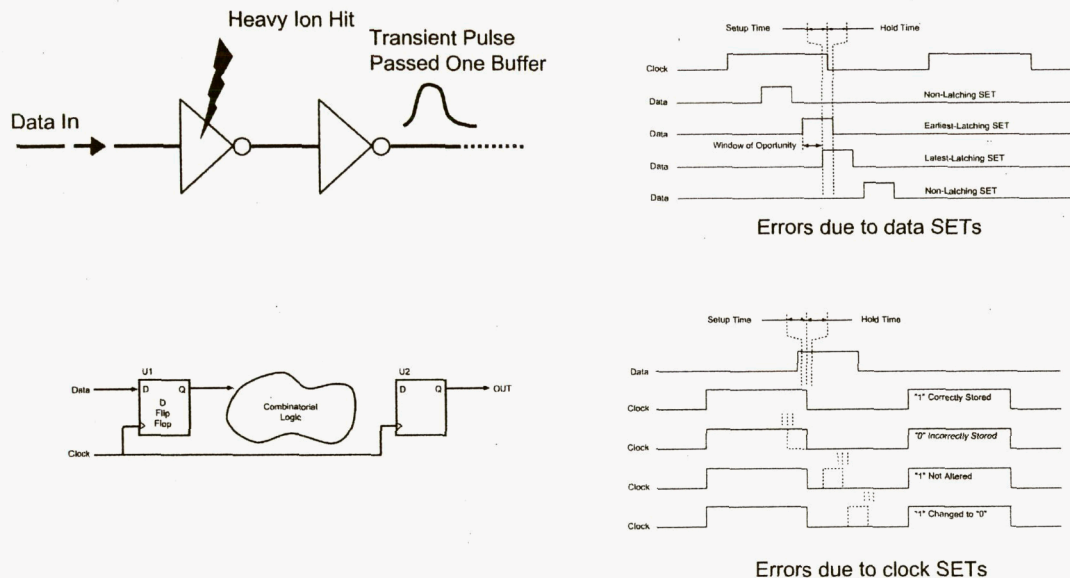
Next, with these issues in mind we will examine present testing capabilities and techniques to identify specific shortfalls and issues.

## 5.1 SEE Testing:

In general SEU testing, including MBU and SEFI characterization, is addressed by two test methods JESD57 and ASTM 1192 that focus on heavy ion testing. Additionally, a test method for SEGR is also available in MILPRF-38535. At present there is not a specific method available at addresses SET.

Recall that an SET is an upset caused by voltage transient engendered in a combinational circuit that propagates to and is latched-in to a storage circuit such that it is mistaken for a real signal or data (Mav) as shown in **Figure 7**.

**Figure 7: SET Errors in Sequential Circuits (Mavis)**

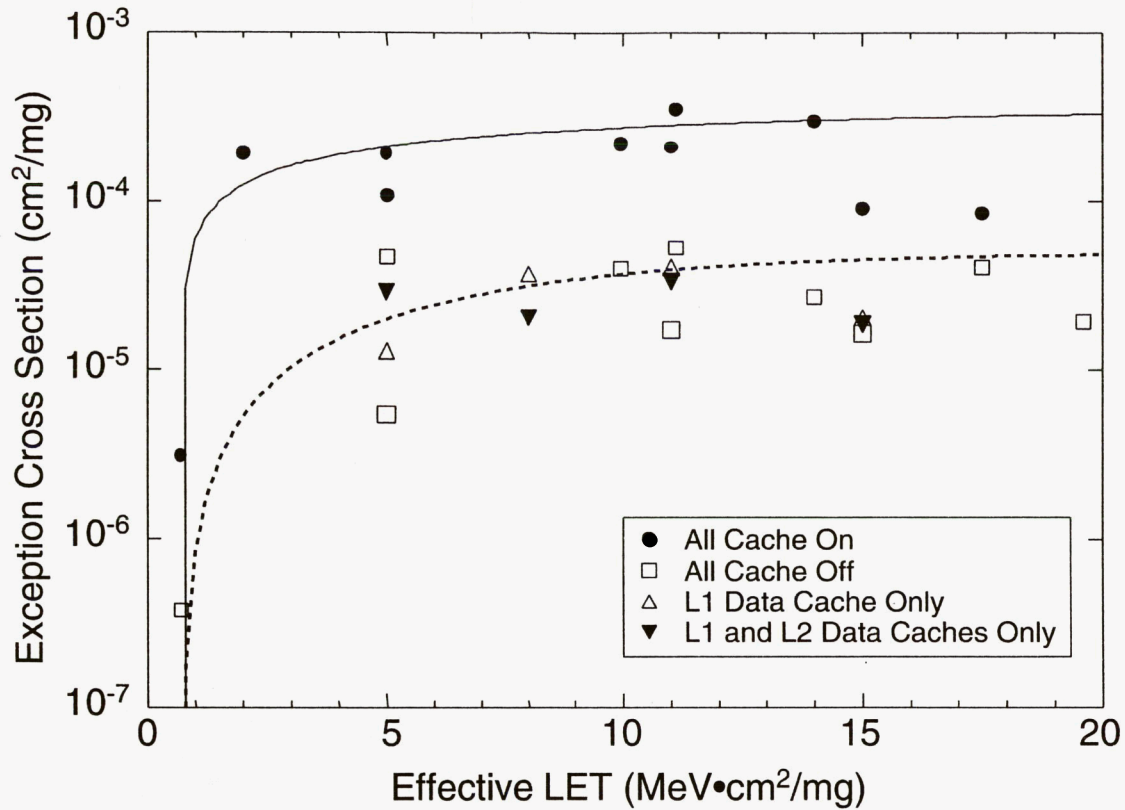


The bulk of the activity has been on SEU testing, however as circuit feature size keeps decreasing, circuit operating speed keeps increasing and suppliers continue to only address SEU hardening in sequential circuits, it is envisioned that SET effects will begin to dominate SEE error-rate response in the near future (Dodd, Mav, Benn, Bau). Thus, it is imperative that SET error-rate prediction and test guidelines be generated in the near future.

The general approach to SEU characterization is well understood, however the issues engendered by circuit sensitivity that are a function of operation mode (e.g. a computation requiring intensive use of cache memory in a microprocessor versus another computation only requiring ALU), operating speed, or other nuances of an IC's operation can be problematic WRT developing accurate error-rate predictions. In **Figure 8** an example of a microprocessor's sensitivity as a function of operating mode is depicted. This issue can be exacerbated if an IC is comprised of different types of circuits (e.g. SRAM, ADC, NVR, etc) which will have significantly different cross-sections and LET's. Such an example is shown in **Figure 9 [BAE or Xilinx data]**.

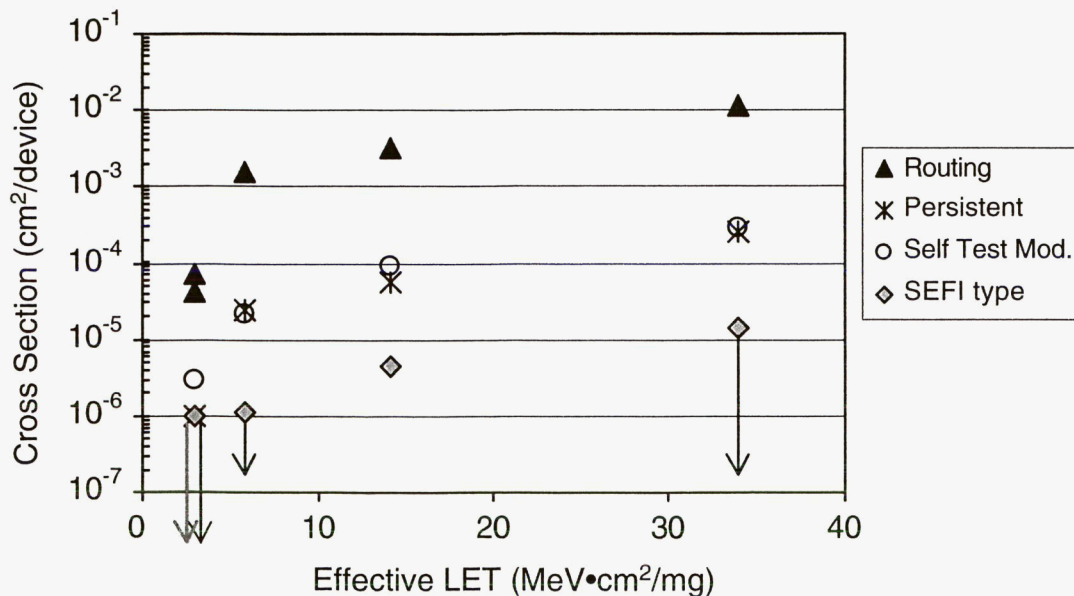
**Figure 8: Pentium III SEFI Heavy Ion Data**

This is a sample of device operating mode SEE sensitivity.



**Figure 9: Configuration Errors in a latch-based (RAM) FPGA**

The complexity of the circuit function provides many different error modes when a configuration bit is altered in these types of devices.



An assessment of the adequacy of SEU/MBU testing and characterization WRT the advanced IC attributes and the relative impact of each attribute is summarized in Table 1, below. Note the affects of increasing intelligence, complexity and virtually all of the other attributes are to worsen SEU/MBU test and characterization.

Moreover, attributes such as construction, packaging and operating speed also influence decision concerning the test facilities and diagnostics that can be used to perform the testing and characterization. Beam energy limitations at Brookhaven National Laboratory, for example limit the type of circuit that can be tested making TAMU and Berkeley National Laboratory the test facilities of choice. Indeed for some devices, depending on the packaging and device configuration higher energy facilities such as National Superconducting Cyclotron Laboratory (NSCL) at MSU and Ganil must be used. In Table 1, the capabilities of the various SEE test facilities generally available are shown as well as their current (March 2005) beam time costs.

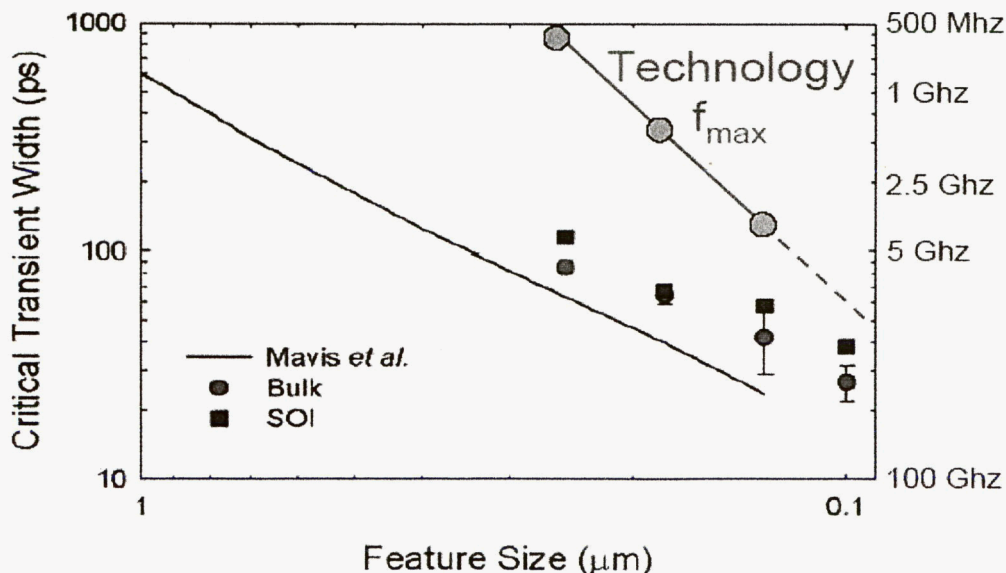
**Table 1: SEE Facility Energy/Range [Reed, et al]**

Insert table

## 5.2 SET Testing and Characterization:

SET testing and characterization represent a relatively new SEE issue. SET was predicted by Mavis (MAV ) and others to occur as circuit feature size scaled below 0.25-microns. At that feature size it was predicted that the un-attenuated propagation of voltage transients, cause by heavy ion strikes, was sufficient to reach a storage (latch) type circuit in the vast majority of circuit designs. Indeed from **Figure 10** that represents the results of modeling by both Dodd and Mavis the propagation length of the transient is considered to be infinite.

**Figure 10: SET Critical Pulse Width for Infinite Propagation**

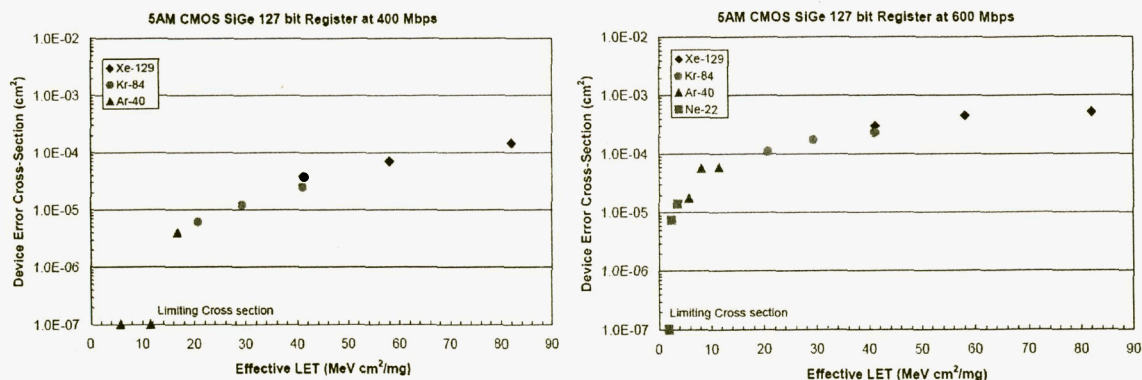


Adapted from P.E. Dodd, et al., "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," IEEE NSREC, 2004.

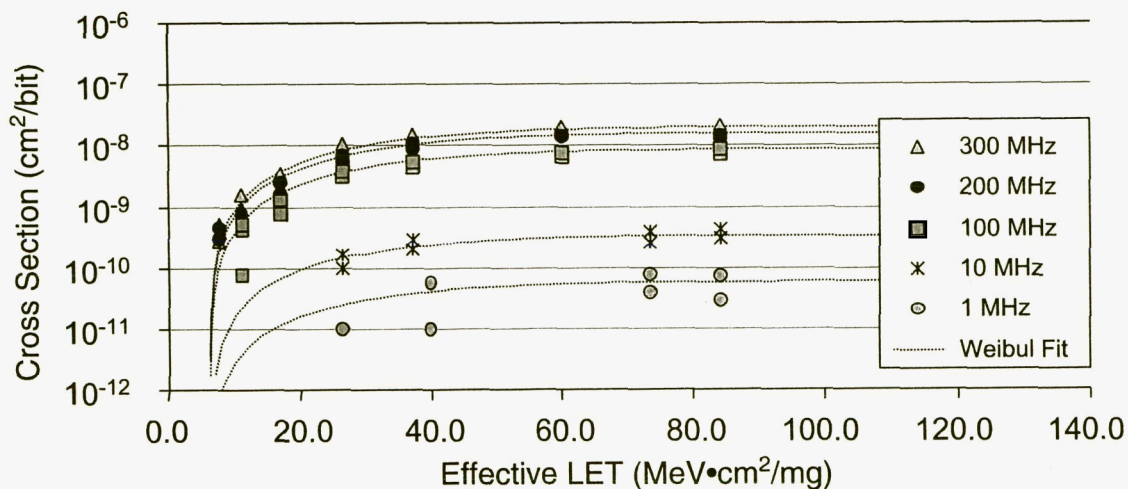
As seen in Figure 11, preliminary work by Marshall, et al [Marshall, TNS] showed an increase in IBM CMOS 5AM device sensitivity to heavy ion strikes as clock speed was increased to greater than 500 MHz with a major increase between the 400-600 MHz regimes. In particular, it is key to note that Marshall, et al have also demonstrated that single particle events can last longer than a single clock cycle (e.g., the pulse generated by a particle strike

approaches 2 nanoseconds, thus when operating frequencies approach 500 MHz, multiple consecutive clock cycles can be corrupted). Further work by Benedetto, et-al (Ben ) has demonstrated the impact of operating frequency on SET error-rate and as can be seen from Figures 12 and 13 a three order of magnitude increase in error-rate can be realized for the DUT when going from 1 MHz to 300 MHz operation for both 0.18-micron and 0.25-micron test structures. Moreover, traditional SEU mitigation methods such as the DICE latch are ineffective in mitigating this effect.

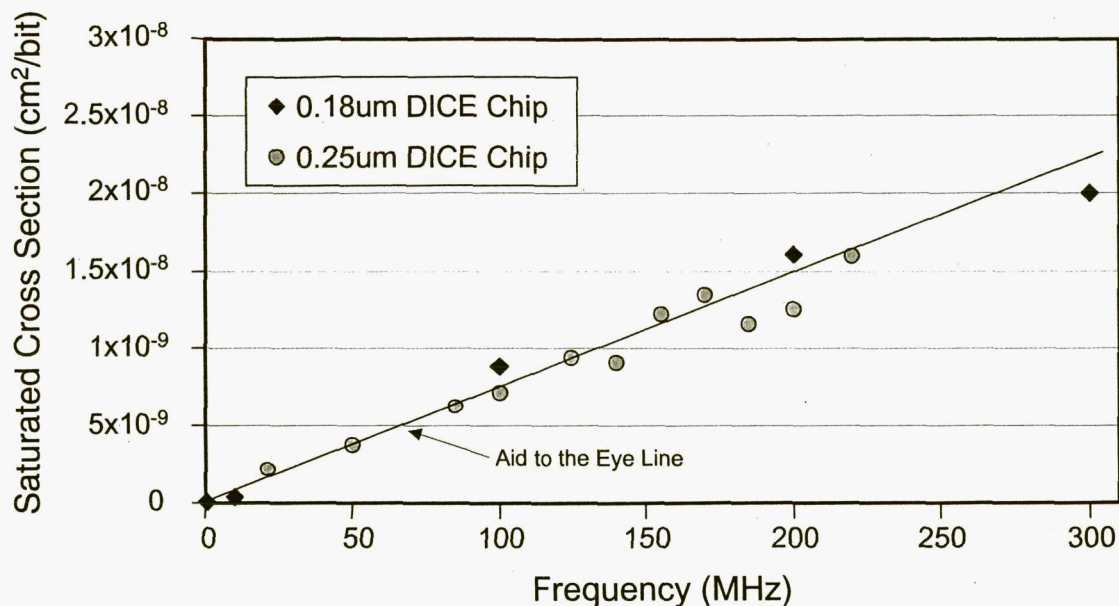
**Figure 11: (Add Fig Caption)**



**Figure 12: 0.18 $\mu$ m DSET Data with Weibull Fits**



**Figure 13: 0.18 and 0.25 $\mu$ m DSET Error Cross Section  
versus Frequency**



More recent testing of deep submicron technologies indicate that this effect may soon become the dominate factor in SEE error-rate generation, especially if circuits fabricated at these feature sizes are hardened against SEU effects.

As previously state there are no test methods or guidelines at present that specifically address SET and the present practice of SEE testing either precludes or makes it extremely difficult to perform testing at system operating speeds. Since testing at speed at present appears to be the only sure method of accurately determining SET error-rates this represents a significant shortfall in our ability to characterize SER in complex IC's where the SER is comprised of both SEU and SET effects. As can be seen from Table 2, SET is exacerbated by most of the IC attributes associated with SEU.

The contrasts between SEU and SET are shown in Table 3.

**Table 2: IC Attribute Impact versus Radiation Test and Characterization**

Attributes	SEU	MBU	SET	SEFI	SEGR	TID
Intelligence	++	++	+	++	-	-
Flexibility	++	++	-	+++	-	+
Complexity	+++	-	+	-	+	++
Integration Density	+	+++	-	-	-	-
Hidden Circuit Features	+	-	-	+++	-	-
Construction	++	++	++	++	++	++
Power	+	+	++	-	-	-
Speed	-	-	+++	-	-	-

+ = worse

++ = much worse

+++ = very significant impact

- = no effect

**Table 3: Comparison of SEU versus SET Mavis, 2001**

- Conventional Static Latch Upset (SEU)
  - Junction collection in static latches & SRAMs
  - Voltage transient magnified by circuit feedback
  - Data state of latch flips if switch point crossed
  - Critical charge decreases as (FS)<sup>2</sup>
- Single-Event-Transients (SET)
  - Junction collection in combinational circuits
  - Voltage transient no longer attenuated in submicron devices
  - Incorrect data latched in at clock edge
  - Critical width for unattenuated propagation decreases as (FS)<sup>2</sup>
  - Error rates increase in proportion to clock frequency

### 5.3 SEFI:

The issues associated with SEFI in complex IC's has been studied for a number of years. Researchers from JPL noted this effect in DRAM technology (SWIFT ) in XXXX. SEFI for this discussion also includes "hang" type responses in microprocessors (Irom) and SRAM based FPGA loss-of-configuration fail modes ( 2000 NSREC SC ). The primary issue with most SEFI events is that the root cause cannot be determined since the critical circuits (registers, logic control, etc.) involved are often not identified by the manufacturer (Hidden Circuit Feature Attribute). Moreover, the ability to reverse engineer these complex IC's to identify root cause problems is prohibitively difficult.

Testing and characterization is a problem since a SEFI event may be operating mode and duty cycle sensitive and only happen when certain interactions between a cache memory and a set of specific registers is occurring. This, of course, places stringent requirements on radiation testing concerning the selection of the DUT operating mode during testing, the selection of the input vectors, and device coverage.

At present there are no guidelines or specific test methods that address SEFI testing and characterization.

#### 5.4 SEGR:

Although SEGR is an issue that has been generally discussed in conjunction with power high voltage semiconductor devices it is also relevant to advanced microelectronics. Specifically, as gate oxide thicknesses continue to follow the scaling rules the potential for a rupture caused by the strike of a single energetic particle becomes more likely. Testing, to-date by Massengill and Sexton, et-al (Wrob 1987, Fisher 1987, Lum 2004, Sexton 1997, Johnston 1998, Sexton 1998, and Mass 2002) have not indicated the existence of an immediate problem, however this is an issue that must remain on our watch-list. Moreover, there is no one test method or guideline that addresses SEGR for low power electronics. A more cogent issue concerning SEGR has to do with the use of drop-in non-volatile memory that use higher than normal operating voltage to implement erase and write functions in large ASIC or SOC devices. For this situation a particle strike during the application of the high voltage has the potential to engender a SEGR event. Moreover, as previously identified for low voltage logic type devices there is no test method or guideline to support users. In addition no body of knowledge is available at this time concerning this failure mode for drop-in Non volatile memory for deep submicron technology.

#### 5.5 TID:

Recent testing (Laoe, NSREC 2003 SC ) has shown that the impact of scaling has served to improve steady state TID performance for low voltage CMOS and HBT technologies. The combination of very thin gate oxides and shallow trench isolation have made it possible to achieve satisfactory TID performance at levels as high as 300 kard.

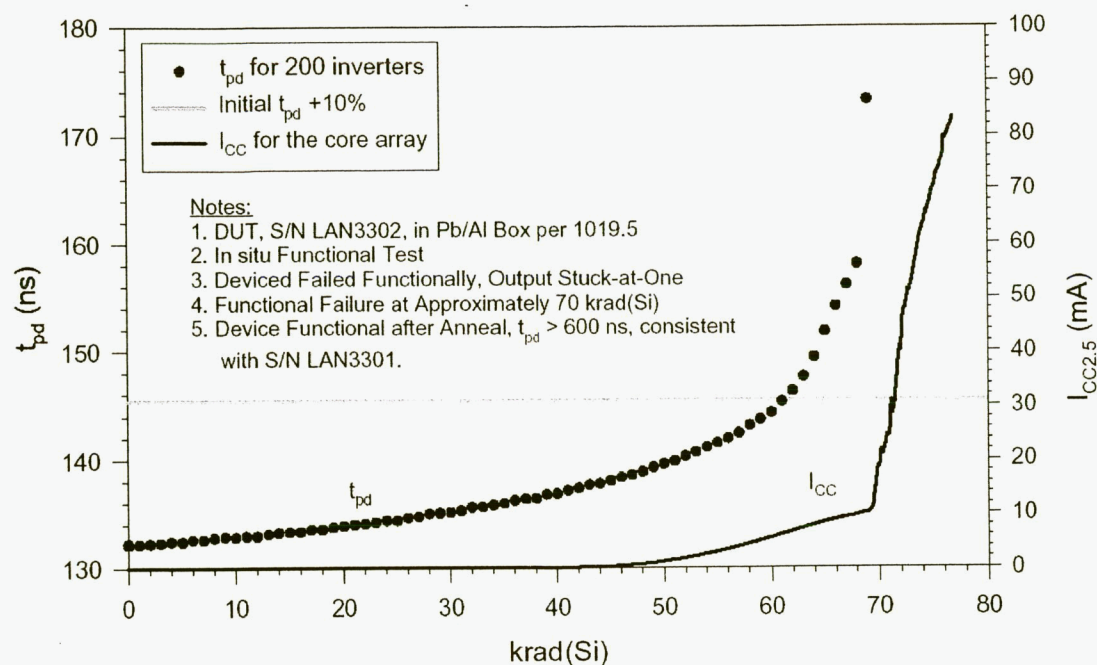
However, several areas still of concern that include:

- Embedded EEPROM programmable drop-ins wherein TID will impact the charge stored on the EEPROM floating gate and has the potential to effect the circuit configuration.
- Embedded programmable drop-ins or other circuits that use charge-pump circuits to develop higher than applied operating voltage potentials to ensure the proper operation of pass-gate devices as shown in **Figure 15**. (JJ Wang TNS Dec 04) [6]

Thus, despite the general improved performance, a TID evaluation of advanced ASIC and SOC devices is required to ensure that "sensitive" sub-circuits are not embedded on the overall low voltage CMOS design.

Additionally, several test method and guideline documents exist to support this type of characterization. add **Ref 1019 1892, esa**) [7]

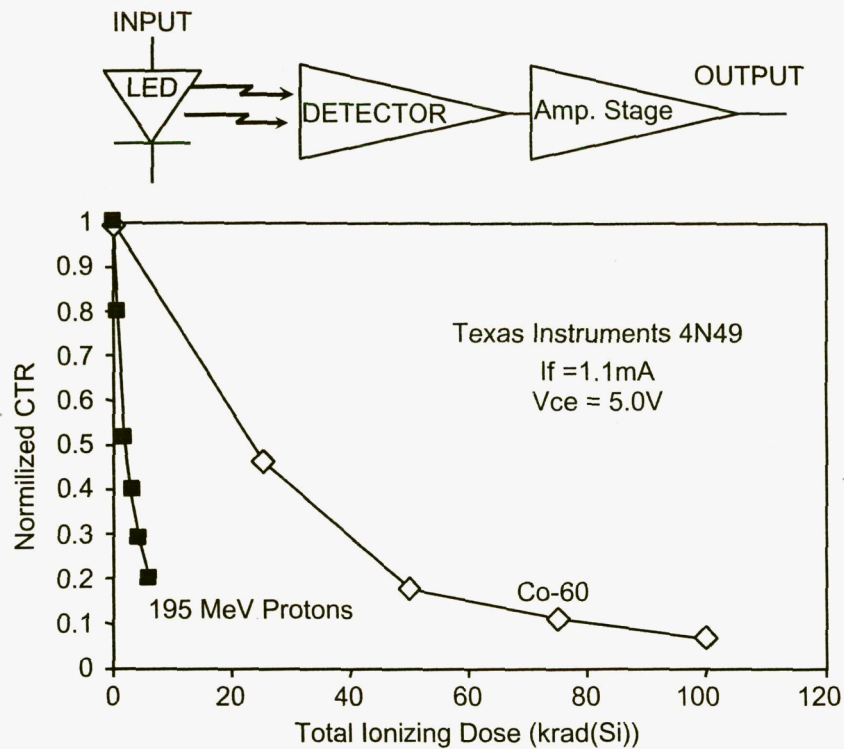
**Figure 15: The impact of total ionizing dose irradiation of the operation of a one-time programmable Actel FPGA utilizing a charge pump circuit**



## 5.6 Displacement Damage Testing and Characterization:

Displacement damage effects have generally not been an issue with either the CMOS or HBT technologies that we can anticipate being used for advanced microelectronics applications. However, with growing use of embedded optoelectronics [REF MIT Mag Silicon Photonics] [8] to facilitate isolation and data transfer applications the need to perform displacement damage testing should be recognized. In a graphic example Johnston, et-al (Joh) demonstrated the danger of neglecting this aspect of flight qualification testing for an optoisolator as shown in **Figure 16**.

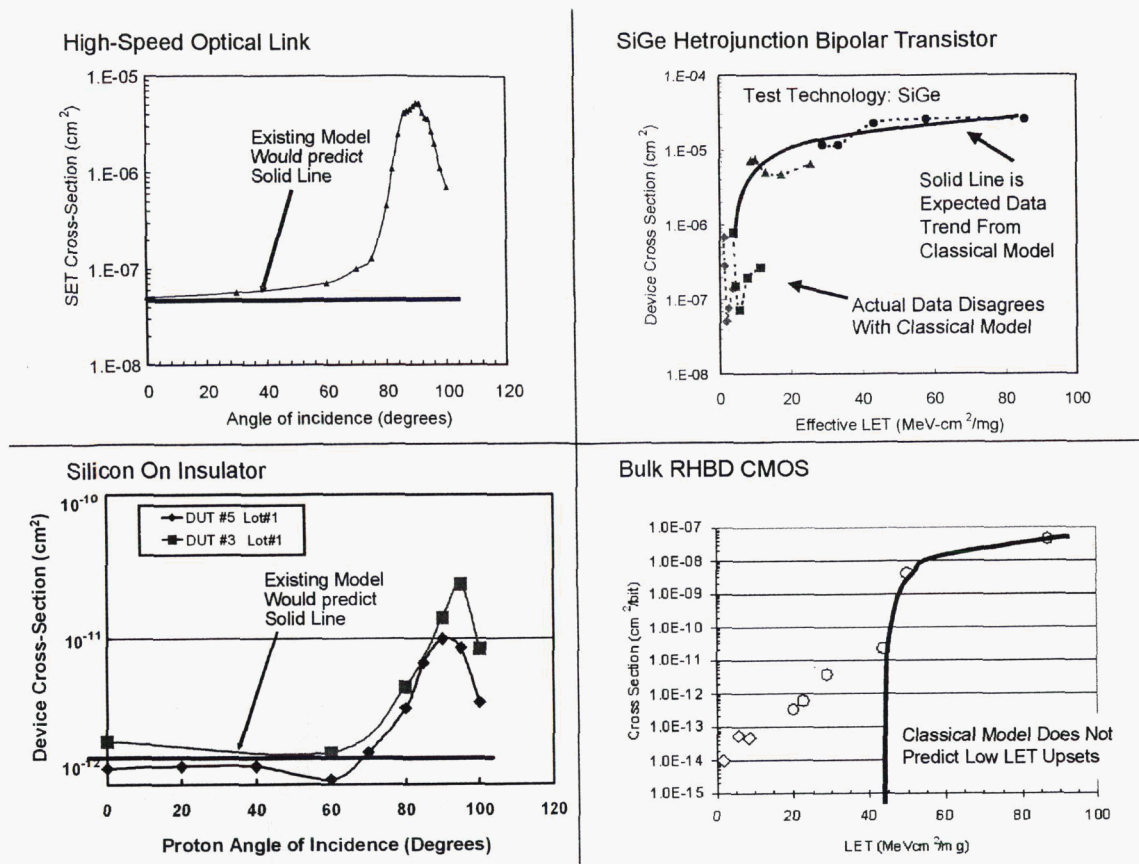
**Figure 16: The effects of Co-60 (gamma) versus proton irradiation on an Opto-Coupler Device high-lighting the effects of displacement damage on Current-Transfer-Ratio (CTR)**



## 5.7 Modeling and Simulation Issues

Radiation response modeling and simulation support for deep submicron technology represents one of the areas where major shortfalls exist. This is a pervasive issue that includes EDA, TCAD, mixed-mode modeling and models that provide an accurate representation of the interaction of energetic particles with deep submicron semiconductor devices including metal over-layer secondary production effects (Reed and Well). Some of the issues with respect to modeling and simulation shortfalls are shown in Figure 17.

**Figure 17: M&S Shortfalls**



## 6 Mitigation Method

A rich body of knowledge exists concerning SEE mitigation and the associated performance, power and area penalties for the various methods. In this section we will examine each of the failure modes described in Sections 3 and 4 and provide a discussion concerning the mitigation methods now in place, their limitations and associated penalties.

### 6.1 SEU and MBU:

SEU/MBU mitigation represents the most widely studied area and vast amounts of effort have gone into the mitigation of this effect. The approaches can be roughly divided into 2 areas that are:

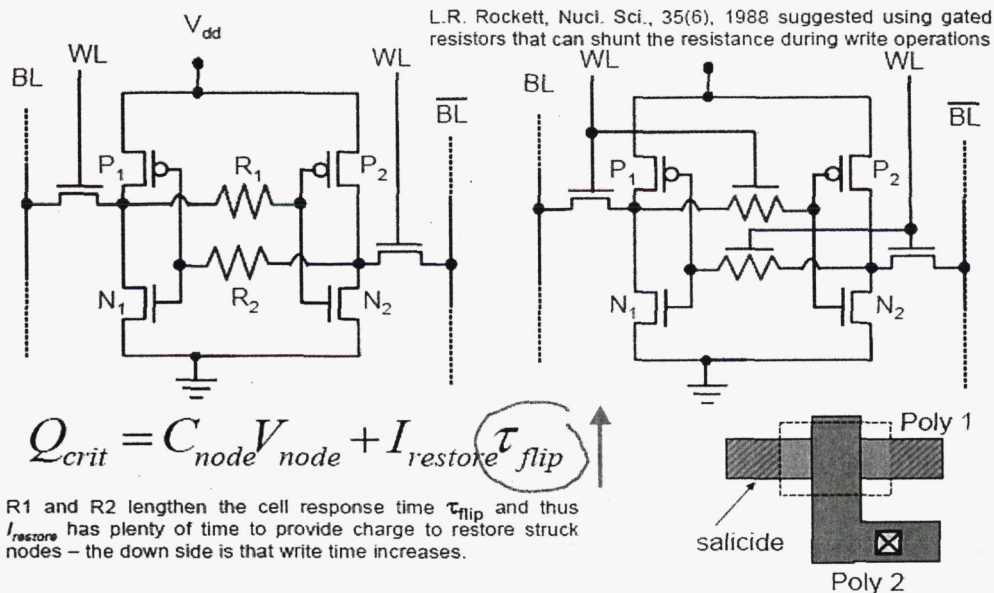
- Process and materials related approaches
- Circuit design and layout related approaches

Additionally, it should be noted that the approaches are often used in layers or combined in various ways.

#### 6.1.1 Process and Layout Approaches:

Concerning process related approaches the one most commonly used is that of the insertion of an RC network into the feedback path for a latch circuit as shown in Figure 18.

**Figure 18: Resistive Hardening SEE Hardening for a Memory Cell**



While this method has been effective in the past there are a number of drawbacks to this approach that include:

- The adverse impact on memory cell write time caused by the RC delay. Note that the use of an electrically gated resistor approach can ameliorate this short coming at the cost of increased circuit complexity. Also, the loss of SEU protection during the write cycle can be construed as a shortfall.
- The issues involved with the use of an RC network include increased process complexity due to the need for a low doped poly-silicon resistor module in the process flow. In addition the positive temperature coefficient associated with the resistor results in a change in SEU immunity across operation temperature range.
- The need too insert a "large " capacitor in the cell can also impact reliability due to issues with oxide integrity, however this has not proved to be a major problem.
- Cell design issues concerning density resulting from the insertion of the RC network. Contemporary approaches have partially resolved this problem by inserting the RC network above the memory cell.

Concerning submicron technologies that can upset at very low charge values the very large resistor value (e.g. > 1Mohms) have made the direct use of this technique difficult since there is a very finite limit to the ohms-square that can be obtained. A method that has been used to extend this approach has been to use it in conjunction with an insulating substrate (e.g. silicon-on-insulator) to reduce charge collection and hence reduce the required resistor size.

Other processing approaches include the use of low resistance epitaxial layers on bulk (or SOI) substrates and /or an insulating substrate to reduce the charge collection volume.

It has been shown that the use of an SOI substrate an order of magnitude decrease in error rate can be achieved over comparable bulk silicon technology.

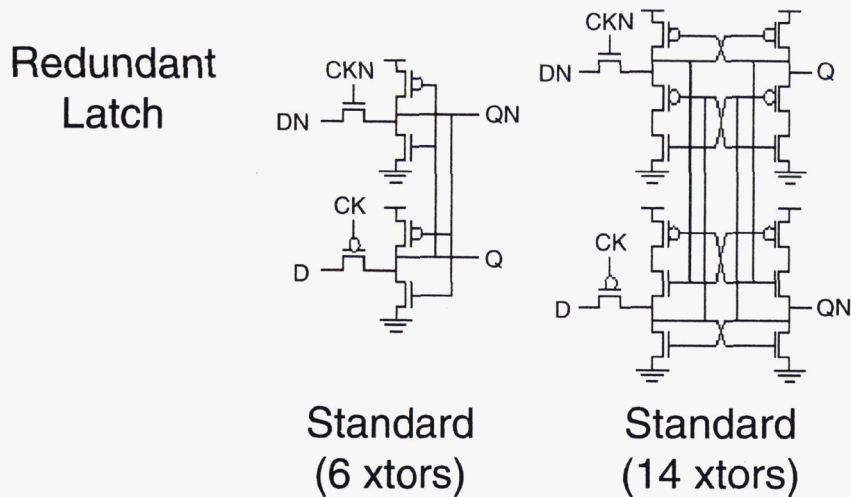
Another processing approach that is also used to achieve improved electrical performance has to do with the use of a retrograde well design where the doping density increases with well depth. The higher doped lower layer serves in much the same way as the above noted epitaxial layer to cut-off the charge track and reduce the collected charge.

Finally, it has been proposed that the use of the retrograde approach be extended to insert a highly doped buried layer to provide a sink for the deposited charge.

### 6.1.2 Circuit Design and Layout Approaches:

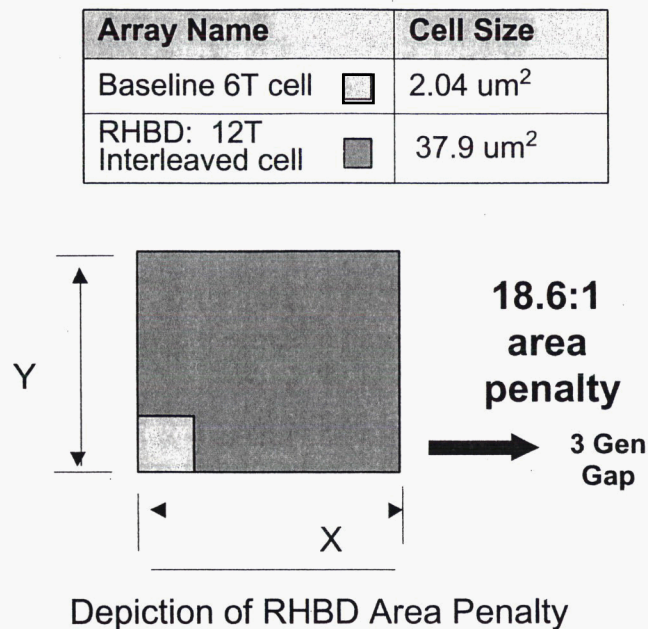
At the circuit design level a number of approaches exist that are all related to the insertion of added transistors in traditional latch designs to preclude cell upset. A number of the design approaches are shown in Figure 19 and include 10 and 14 transistor memory cells and other such configurations.

**Figure 19: Circuit Design Approaches**



The benefits of a design approach in general relate to their ability to be assimilated into almost any fabrication process and supported by standard design libraries. However, the related area and power penalties associated with this approach are significant as demonstrated in Figure 20 that compares a 12T memory cell with a 6T cell (Ref) [9]. Thus, while effective in suppressing SEU this approach does not necessarily lend itself to the fabrication of high-density memory devices.

**Figure 20: RHBP versus Pure RHBD Performance Comparison; DARPA RHBD Program , March 2005**



Other less obvious problems with above note approaches include the fact that upset is not precluded if multiple nodes are struck and the designs do not address SET mitigation.

Two layout approaches that are often used concurrently with these design approaches include the use of word bit physical location staggering and critical node interleaving.

The placement of bits within the same word in physical locations that preclude being struck by a single ion is an approach that support EDAC by limiting the corrections to single vice multiple bits and thus simplifying correction and detection circuit design.

Critical node inter-leaving refers to the layout practice of placing nodes within a cell in locations that preclude or at least significantly reduce the probability of a multiple node strike that can obviate the effectiveness of these design approaches as shown in Figure 21.

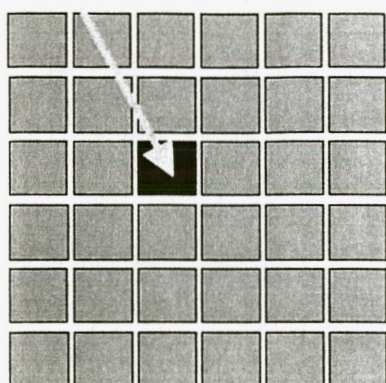
At a higher level of integration density techniques that include, but are not limited to, error-correction and detection and voting through triple or more modular redundancy can be employed. EDAC methods come in many shapes and sizes and include a variety of algorithms such as Hamming Code, Reed-Solomon, etc., but each of these must be evaluated versus word length, latency, circuit complexity, area, power, etc [Heidergott, NSREC SC 2002 or 3] [10].

The negative impacts of EDAC and voting can be summarized as:

- Additional circuitry that impacts power and density
- The need to periodically scrub the protection circuits to eliminate latent errors that result in increased system design complexity.
- Reductions in system throughput due to the increased circuit levels needed to implement these methods.

In closing, there are a number of techniques that can be applied to mitigate SEU/MBU and, depending on system availability requirements, these approaches can be applied in a layered manner to achieve operating goals.

**Figure 21: SEU versus MBU (Bauman) IEEE Short Course 2005**

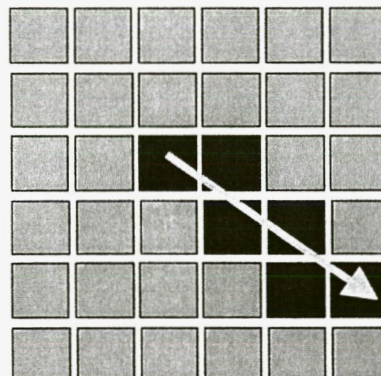


### Single Bit Upset

Transient induces change in the voltage of a storage node (injects a current) that is sufficient to defeat the circuit feedback holding the data state such that the data state is reversed.

### Multiple Bit Upset

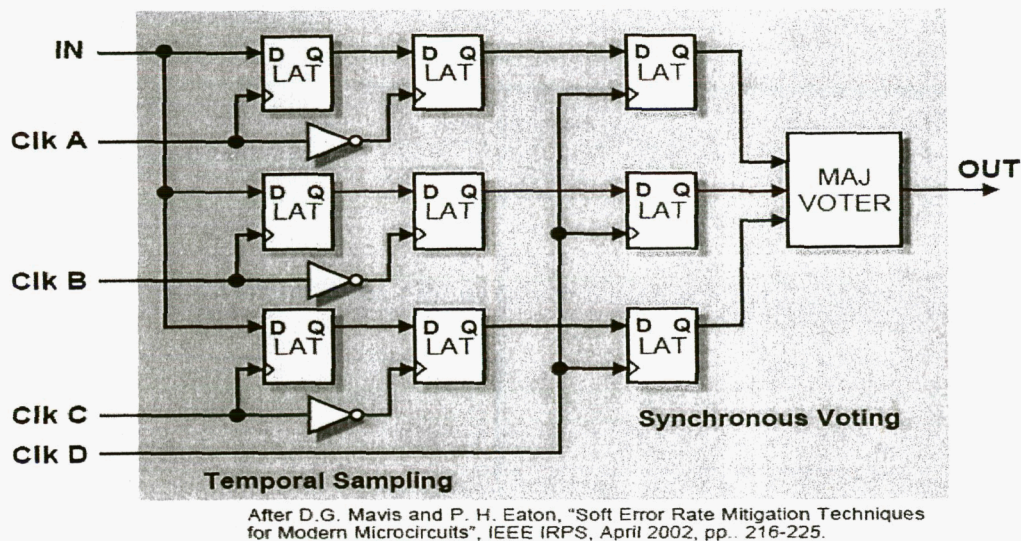
Same mechanism as SBU except the radiation event has higher charge density and/or a larger range such that multiple bits are upset by the single event.



## 6.2 SET:

At present the basic approach to mitigate SET involves the use of a circuit denoted at the Temporal Latch, as shown in Figure 22 (Ref) [11] that in essence is a TMR circuit aligned to compare voltage transients that can be separated as a function of pulse width. Specifically, the method depends on a fairly precise knowledge of the transient pulse width and the ability to operate the circuit (or system) at speeds that allow one to use a pulse width that is  $\sim 2X$  the transient pulse width. Thus, if a transient pulse created from an ion strike is measured for a technology to be 1ns the maximum operation speed of the system would be limited to 500 Ghz. Obviously such a limitation could impose onerous restrictions on system operation. SET effects have not been analyzed to the extent of SEU since it has only become a problem as feature size has been scaled to  $< 0.25$ -microns. Above this feature size the transient induced pulse widths were insufficiently wide to allow for significant stage-to-stage propagation and thus were not evident. However, as seen from Figures 12 and 13 (Mav and Ben) this is no longer the case.

**Figure 22: SET & SEU Hardened Latch (Temporal Latch)**



In addition to the circuit design mitigation approach any or all of the processing approaches that reduce charge collection volume would be appropriate to reduce the amplitude and width of the voltage transient caused by the energetic particle strike.

### 6.3 SEFI:

In principle, all of the techniques available to mitigate SEU effects are appropriate for SEFI, with the exception of EDAC and thus, SEFI mitigation should be a generally straight forward issue. However, this is seldom the case since a SEFI response is usually the result of some unidentified part of a complex circuit being upset and the user has little or no insight into the root cause of the response. Moreover, obtaining this level of information from the manufacturer is not viable. Additionally, for complex microprocessors the SEFI or "Hang" response can be a function of the immediate operation of the circuit, e.g. interaction between the application program, specific computation and cache memory, making the mitigation of the SEFI all but impossible. SRAM based reconfigurable FPGA devices can also fall victim to a SEFI that inadvertently reconfigures the programmed architecture.

Concerning SEFI mitigation for standard IC's system level approaches such a "Watch-Dog" timers, frequent critical circuit configuration bit comparisons, scrubbing and other external approaches can be used.

However, as previously noted these external monitoring and control circuits must be radiation hardened and add to system overhead.

### 6.4 SEL:

The mitigation of SEL can also be delineated into (1) a process and materials approach and a (2) design and layout approach.

Concerning processing and material the use of an insulating substrate or an epitaxial layer to impact the parasitic bipolar transistors operation have been used effectively in the past. The insulating layer eliminates the formation of the SCR circuit. The low resistance epitaxial layer prevents the SCR from turning on by shunting the base resistor with a low impedance path for the charge and thus the SCR never goes into forward bias and Latch-up.

Concerning design and layout the use of a guard ring around each CMOS device interrupts the SCR structure precluding turn-on. Additionally, by increasing well spacing the combined gain if the parasitic transistors can be reduced to eliminate latch-up.

The approaches to SEL mitigation has been widely discussed and can be found in Refs [12].

The impact of these mitigation methods either involves an increase in process complexity or some area penalty to insert either a guard ring of separate the n-channel and p-channel transistors.

## **7 Recommendations:**

Thus, based on the discussion of Section 5.0, a number of recommendations concerning areas that require additional support are provided as follows:

- Improved understanding extreme value statistics as it applies to radiation particle impacts
- Development of High-Energy SEU Micro-beam [REF: Ladbury SEE Symp 04] [13] and TPA Laser [McMorrow, TNS 04] [14]
- Development and validation of System Risk Tools
- Development of Portable High-Speed Device Testers
- Development of Physics Based Modeling Tool and an efficient mixed-signal modeling capability [REF: Schrimpf, HEART 05] [15]
- Development of substrate engineering processing methods to decrease charge generation and enhance recombination.

While it is not suggested that the availability of these methods will provide a panacea concerning the resolution of the issues identified in Section 5.0 it is envisioned that they will provide a foundation to support the use of advanced deep submicron microelectronics for high reliability space applications.

## **8 Summary and Conclusions**

Concerning the areas of testing, modeling and simulation a number of shortfalls and/or deficiencies with our present capabilities can be identified. These would include the absence of dedicated test methods and guideline documents as well as limitations concerning modeling and simulation of both SEE and TID in these ultra-deep submicron technologies. These issues have been discussed in some detail in the preceding sections and are summarized in the Table 4, below.

**Table 4: Summary of testing and modeling and simulation support for Advanced Microelectronics**

Radiation Response	Guideline Document	Test Method	Data Base	Modeling & Simulation
SEU/MBU	Yes	Yes	Yes	~ mature
SET	No	No	No	No
SEL	Yes	Yes	Yes	No
SEGR	No	No	No	No
SEFI	No	No	No	No
TID	Yes	Yes	Yes	Yes
Displacement Damage	Yes	Yes	No	No

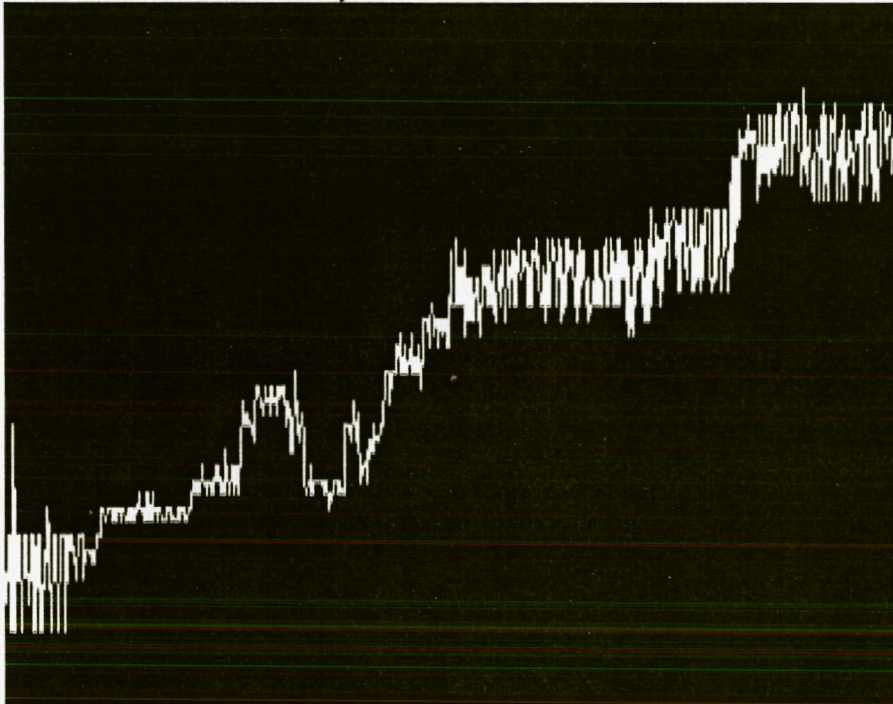
As can be seen and inferred from the number of areas that are shaded red there are significant shortfalls concerning our ability to support testing and model and simulate the most of the effects of radiation induce degradation of these technologies. Moreover, in man cases there is a lack of test data to support space applications.

In addition, an examination of the presently available and well understood mitigation methods reveals that the majority involve penalties in both area and power that significantly erode the performance and integration density improvements afforded through the use of advanced microelectronics technologies.

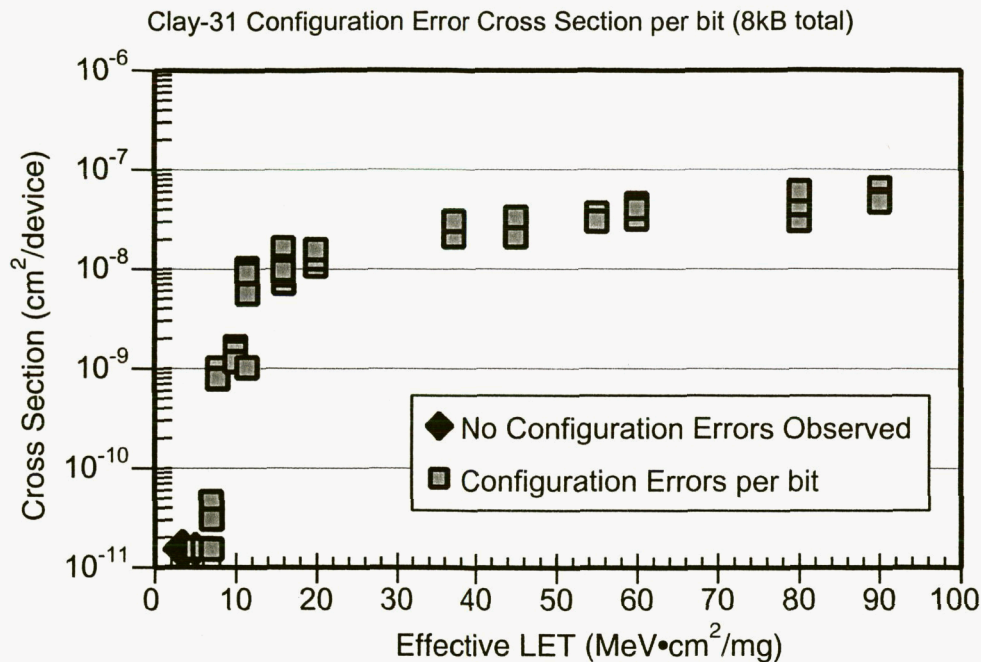
Moreover, from the discussion of Section 5.0 on modeling and simulation, we note that there are also profound issues concerning the present fidelity of our simulation capabilities.

**Figure TBD: Clay-31 CSRAM FPGA  
SEU Impact on Configuration Signature**

Heavy Ion Irradiation time in mS



**Figure TBD: SER – Single Event Reprogramming**



## 9 References:

- [1] NASA/GSFC Radiation Effects and Analysis home page, <http://radhome.gsfc.nasa.gov>
- [2] Benedetto IEEE TNS04 or SEE Symp04
- [3] REF Farok Iron (Memory devices and microprocessors with multi-threading capability further increasing issues with SEFI and SEFI mitigation)
- [4] ref JPL NASA doc (Plastic encapsulation has significantly complicated device SEE test preparation since removal without damaging the DUT can be a time consuming and difficult endeavor.)
- [5] REF Schrimpf/Reed/Weller HEART 05 (As previously stated the disparity of the results between modeled and measured SEE response)
- [6] J. J. Wang, et al., "Total Dose Radiation Effects on Flash-based FPGA," TNS Dec 04, 190-195.
- [7] Ref 1019 1892, esa (Additionally, several test method and guideline documents exist to support this type of characterization.)
- [8] REF MIT Mag Silicon Photonics (Displacement damage effects have generally not been an issue with either the CMOS or HBT technologies that we can anticipate being used for advanced microelectronics applications. However, with growing use of embedded optoelectronics)
- [9] REF (the related area and power penalties associated with his approach are significant as demonstrated in Figure 20 that compares a 12T memory cell with a 6T cell)
- [10] REF (Heidergott, NSREC SC 2002 or 3 - EDAC methods come in many shapes and sizes and include a variety of algorithms such as Hamming Code, Reed-Solomon, etc., but each of these must be evaluated versus word length, latency, circuit complexity, area, power, etc)
- [11] REF (At present the basic approach to mitigate SET involves the use of a circuit denoted at the Temporal Latch, as shown in Figure 22)
- [12] REF (The approaches to SEL mitigation has been widely discussed and can be found in Refs)
- [13] REF (Ladbury SEE Symp 04)
- [14] REF (McMorrow, TNS 04)T.F Wrobel, IEEE-TNS, vol 34, pp1262-1268, 1987
- [15] REF: Schrimpf, HEART 05